In The Specification:

Please replace the paragraph beginning on page 10, line 6 with the following amended paragraph.

Continuing with Fig. 2, a self-aligned metal silicide (SALICIDE) layer 22 is formed on the polysilicon gate electrodes 14 and on the source/drain contact areas 20. The SALICIDE is formed by depositing a metal, such as cobalt (Co), nickel (Ni), and titanium (Ti), on the exposed polysilicon gate electrodes 14 and on the source/drain contact areas 20 and annealing to form CoSi. The SALICIDE layer is formed to a thickness of between about 250 and 400 Angstroms. Then the unreacted Co on the insulating surfaces (not shown) is removed. As described in detail above, in the conventional process for very-high density circuits with minimal feature sizes, the aspect ratio of the spacings or gaps G1 between the gate electrodes having sidewall spacers can be very large (for example, greater than 5). As shown in the prior-art in Fig. 1, these high aspect ratio gaps can result in void formation V during subsequent ILD layer deposition 24.

Please replace the paragraph beginning on page 10, line 22 with the following amended paragraph.

Referring to Fig. 3, a novel feature of this invention is to remove the sidewall spacers 18, which increases the spacings or gaps between the FED gate electrodes, thereby reducing the aspect ratio of the spacing or gaps, labeled G2. For example, the aspect ratio can be reduced from 5.0 to less than 1.5 or about 1.4. The Si_3N_4 sidewall spacers 18 are selectively removed preferably using a hot H_3PO_4 etch. Alternatively the sidewall spacers can be removed using in-

situ plasma etching in a high-density plasma (HDP) etcher. After removing the sidewall spacers 18, the remaining CoSi 22 on the gate electrodes 14 and on the source/drain contact areas 20 is retained to provide low contact resistance during subsequent processing.